ABSTRACT

A method and circuit for transferring multiple bits of data across asynchronous clock domains is provided. The method includes detecting a change in a status bit of a data word being transferred from a source in a source clock domain to a destination register in a destination clock domain, the source clock and destination clock being asynchronous. The method includes sampling the detected change in reference to a change window where the change window is sized to encompass all bits of the data word. A stable input is selected for each bistable circuit of the destination register based on whether the detected change in the status bit is likely to produce metastability in the receiving register.